

## Section 19 E Clock Interface

### 19.1 Overview

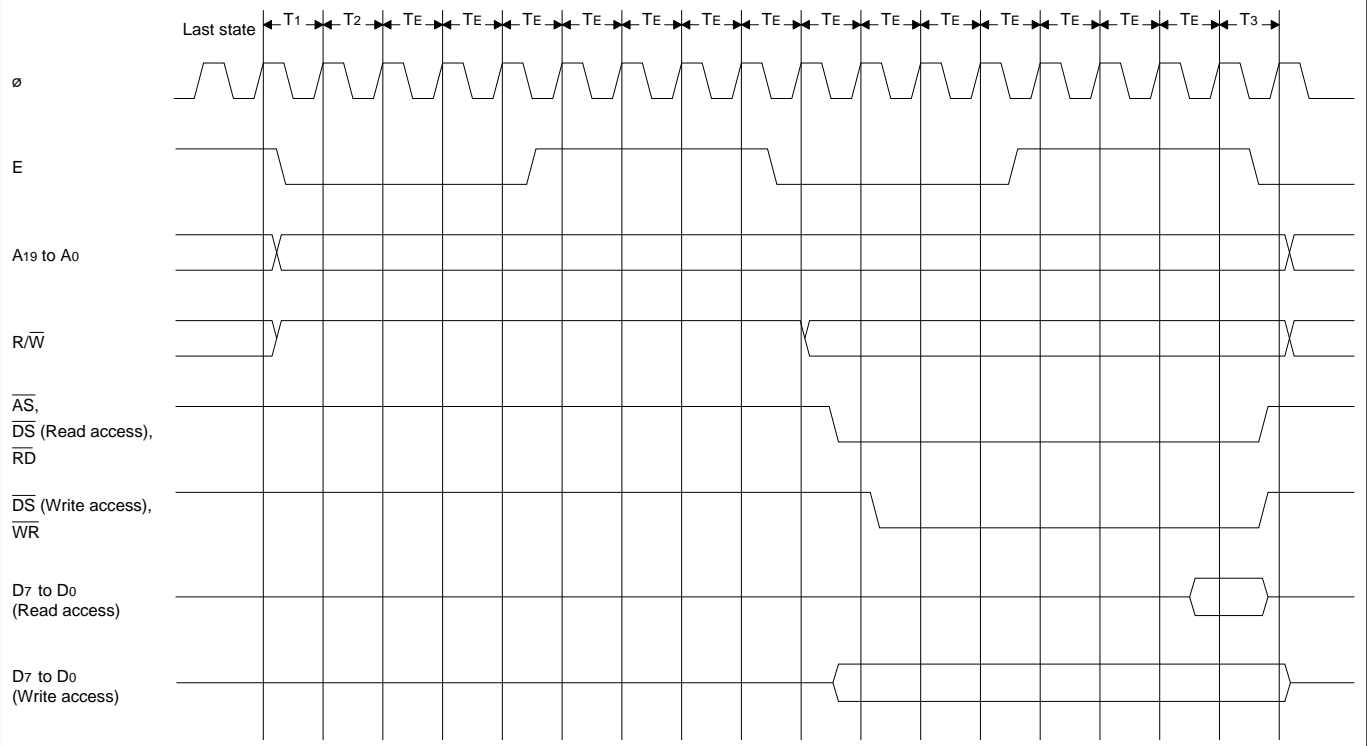
For interfacing to E clock based peripheral devices, the H8/532 can generate an E clock output. Special instructions (MOVTPE, MOVFPE) perform data transfers synchronized with the E clock.

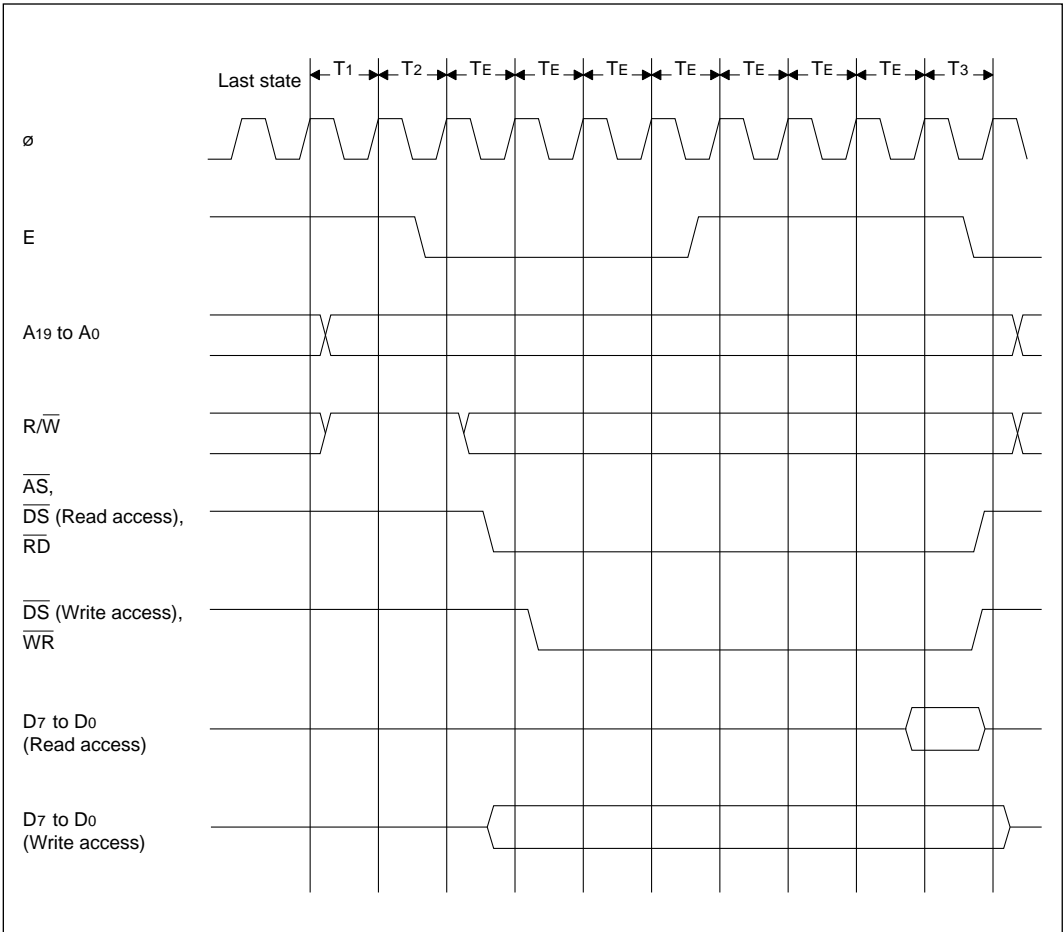
The E clock is created by dividing the system clock ( $\phi$ ) by 8. The E clock is output at the P11 pin when the P11DDR bit in the port 1 data direction register (P1DDR) is set to 1.

When the CPU executes an instruction that synchronizes with the E clock, the address is output on the address bus as usual, but the data bus and the  $\overline{R/W}$ ,  $\overline{DS}$ ,  $\overline{RD}$ , and  $\overline{WR}$  signal lines do not become active until the falling edge of the E clock is detected. The length of the access cycle for an instruction synchronized with the E clock is accordingly variable. Figures 19-1 and 19-2 show the timing in the cases of maximum and minimum synchronization delay.

The wait state controller (WSC) does not insert any wait states ( $T_w$ ) during the execution of an instruction synchronized with the E clock.

**Figure 19-1 Execution Cycle of Instruction Synchronized with E Clock in Expanded Modes (Maximum Synchronization Delay)**





**Figure 19-2 Execution Cycle of Instruction Synchronized with E Clock in Expanded Modes (Minimum Synchronization Delay)**